WHAT IS CLAIMED IS:

1. A metal alloy interconnect used in semiconductor devices comprising:

an intermediate layer of the metal alloy interconnect on a dielectric material, the intermediate layer having a relatively higher concentration of an impurity metal along with a primary metal,

a main layer of the metal alloy interconnect on top of the intermediate layer and surrounded by the intermediate layer, the main layer having a relatively higher concentration of the primary metal than the intermediate layer;

wherein the intermediate and main layers of the metal alloy interconnect each maintains a material uniformity.

2. The metal alloy interconnect of claim 1 wherein the primary metal is Cu.

3. The metal alloy interconnect of claim 1 wherein the impurity metal is Sn or Tin.

4. The metal alloy interconnect of claim 1 further comprising a seed layer underneath the intermediate layer, the seed layer having pure primary metal.

5. The metal alloy interconnect of claim 1 wherein the main and

intermediate layers of the metal alloy interconnect have a coplanar surface.

6. A method for fabricating a metal alloy interconnect in a semiconductor device, comprising:

defining a metal alloy interconnect boundary profile on a substrate material;

subjecting the substrate material to a first wet process for fabricating an intermediate layer of the metal alloy interconnect conforming to the boundary profile;

subjecting the substrate material having the intermediate layer to a second wet process for fabricating a main layer of the metal alloy interconnect containing a primary metal,

wherein the intermediate layer has a relatively higher concentration of a secondary metal than the main layer.

7. The method of claim 6 wherein the first and second wet process includes at least one electro-chemical plating process.

8. The method of claim 6 wherein the first and second wet process includes at least one electroless plating process.

9. The method of claim 6 wherein the first wet process is controlled by using a relatively high bias voltage to create the relatively higher concentration of the secondary metal.

10. The method of claim 6 wherein the second wet process is controlled by using a relatively low bias voltage to maintain a relatively low concentration of the secondary metal.

11. The method of claim 6 wherein the first and second wet processes are further enhanced by adjusting plating temperatures in the processes, thereby adjusting a thermal budget for fabricating the metal alloy interconnect.

12. The method of claim 6 wherein the primary metal is Cu.

13. The method of claim 6 further comprising fabricating a seed layer before fabricating the intermediate layer so that the seed layer is underneath the intermediate layer.

14. The method of claim 13 wherein the seed layer has pure primary metal.

15. The method of claim 6 further comprising employing a chemical-mechanical process to form a coplanar surface of the intermediate and main layers.

16. A Cu alloy interconnect used in semiconductor devices comprising:

a seed layer having pure Cu formed on a boundary profile in a substrate material;

an intermediate layer over the seed layer;

a main layer of the Cu alloy interconnect over and surrounded by the intermediate layer,

wherein the intermediate layer and the main layer of the Cu alloy interconnect each maintains a material uniformity, wherein the intermediate layer has a relatively higher concentration of an impurity metal than the main layer.

17. The Cu alloy interconnect of claim 16 wherein the intermediate layer is in contact with a non-metal portion of the semiconductor device.

18. The Cu alloy interconnect of claim 16 wherein the impurity metal is Sn.

19. The Cu alloy interconnect of claim 16 wherein the impurity metal is Tin.

20. The Cu alloy interconnect of claim 16 wherein the main and intermediate layers have a coplanar surface.